

U.S. Department of Commerce, Patent and Trademark Office <div style="border: 1px solid black; border-radius: 50%; padding: 10px; width: 100px; float: left; margin-right: 10px;"> OFFICE MAY 23 2006 PATENT & TRADEMARK OFFICE </div> RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)				Docket No.: 8201/Y01/SYNX/JW		Serial No.: 10/764,620	
				Applicants: Michael R. Rice, et al			
				Filing Date: January 26, 2004		Group: 2125	

U.S. Patent Documents							
*Examiner Initial	Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate	
	US-1						
	US-2						
	US-3						
	US-4						
	US-5						
	US-6						
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	US-8						
	US-9						
	US-10						
	US-11						

Foreign Patent Documents							Translation	
	Document Number	Date	Country	Class	Subclass	Yes	No	
CK	F-1	JP 08249044 A	09/27/96	Japan		X		
CK	F-2	JP 09115817 A	05/02/97	Japan		X		
CK	F-3	JP 10135096 A	05/22/98	Japan		X		
CK	F-4	JP 11176717 A	07/02/99	Japan		X		
CK	F-5	JP 11296208 A	10/29/99	Japan		X		

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
CK	OT-1	Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)
CK	OT-2	Juba, R. C. et al., "Production improvements using a forward scheduler", 1996, Seventeenth IEEE/CPMT International Electronics Manufacturing Technology Symposium 'Manufacturing Technologies - Present and Future', Pg. 205-9.
CK	OT-3	Houmin, Yan et al., "Testing the robustness of two-boundary control policies in semiconductor manufacturing", May 1996, IEEE Transactions on Semiconductor Manufacturing, Vol. 9 No. 2, Pg. 285-8.

Examiner <i>Chait Kuy</i>	Date Considered 7/31/06
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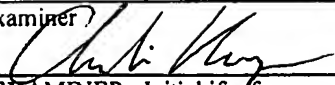
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CK	F-6	JP 2001332464 A	11/30/01	Japan			X	
CK	F-7	JP 2003007584 A	01/10/03	Japan			X	
CK	F-8	DE 19715974 A1	10/22/98	Germany			Abstract	
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	F-10							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
CK	OT-4	Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.
CK	OT-5	Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.
CK	OT-6	Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.

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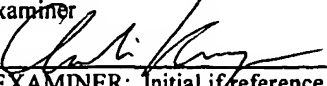
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	F-12							
	F-13							
	F-14							
	F-15							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
CK	OT-7	Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags YASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.
CK	OT-8	Wei Jun-Hu et al., "Optimization methodology in simulation-based scheduling for semiconductor manufacturing", Oct. 2000, Information and Control, Vol. 29 No. 5, Pg. 425-30, Chinese language. (Abstract only)
	OT-9	

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